

FIG. 1

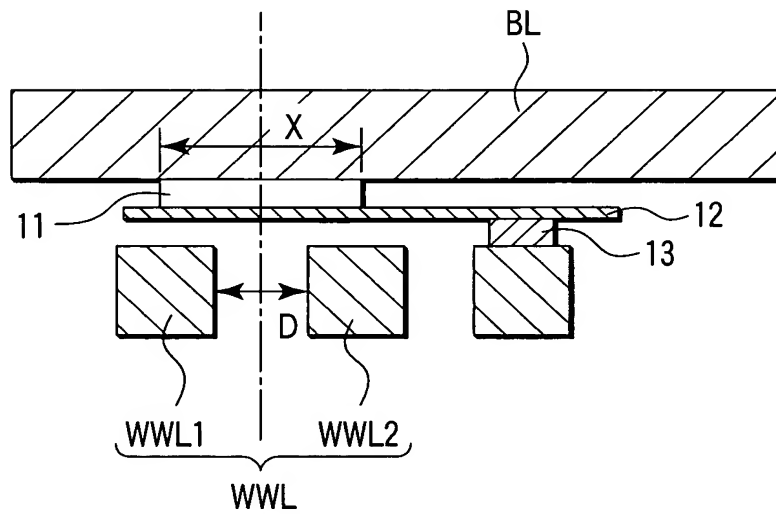


FIG. 2

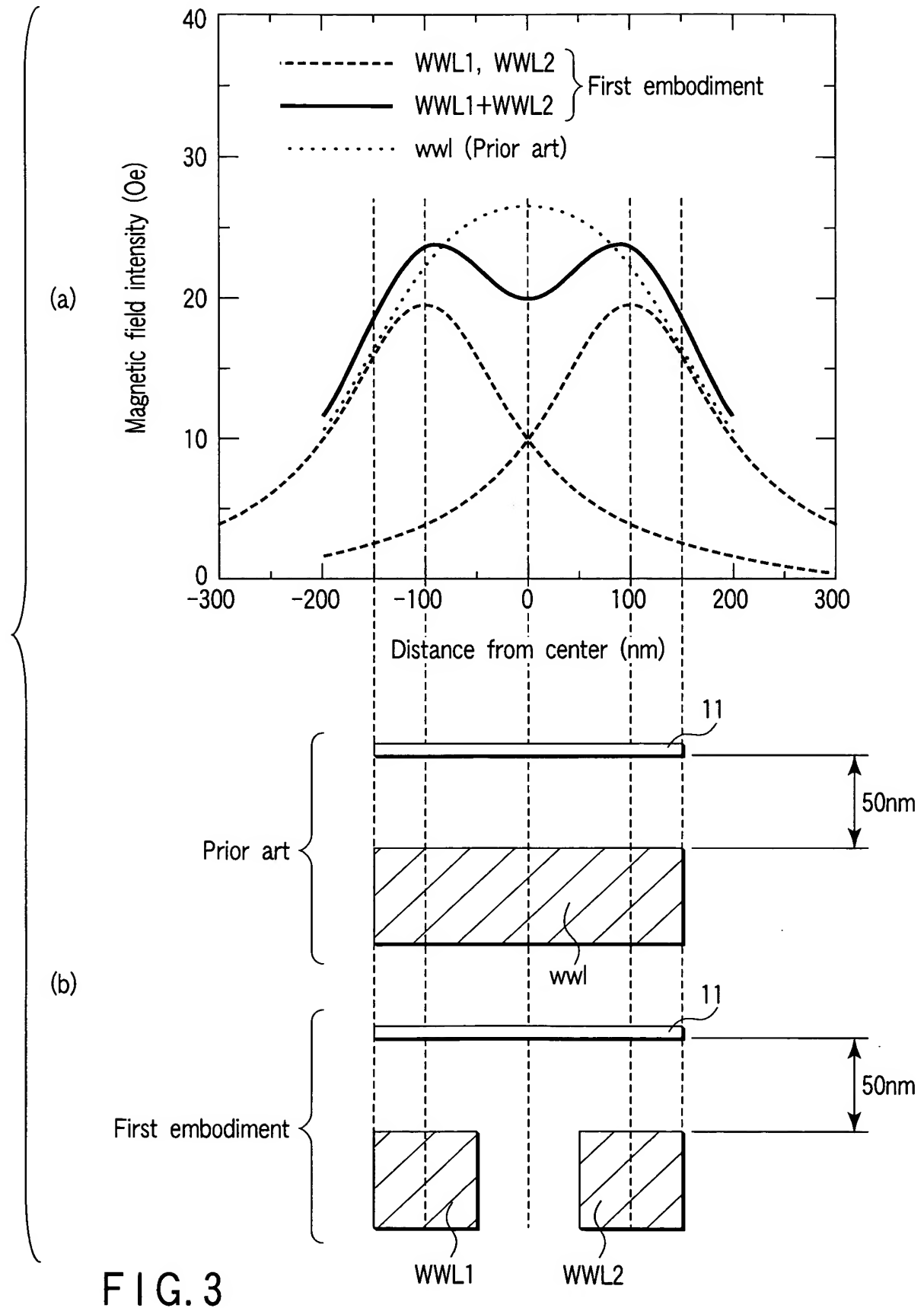


FIG. 3

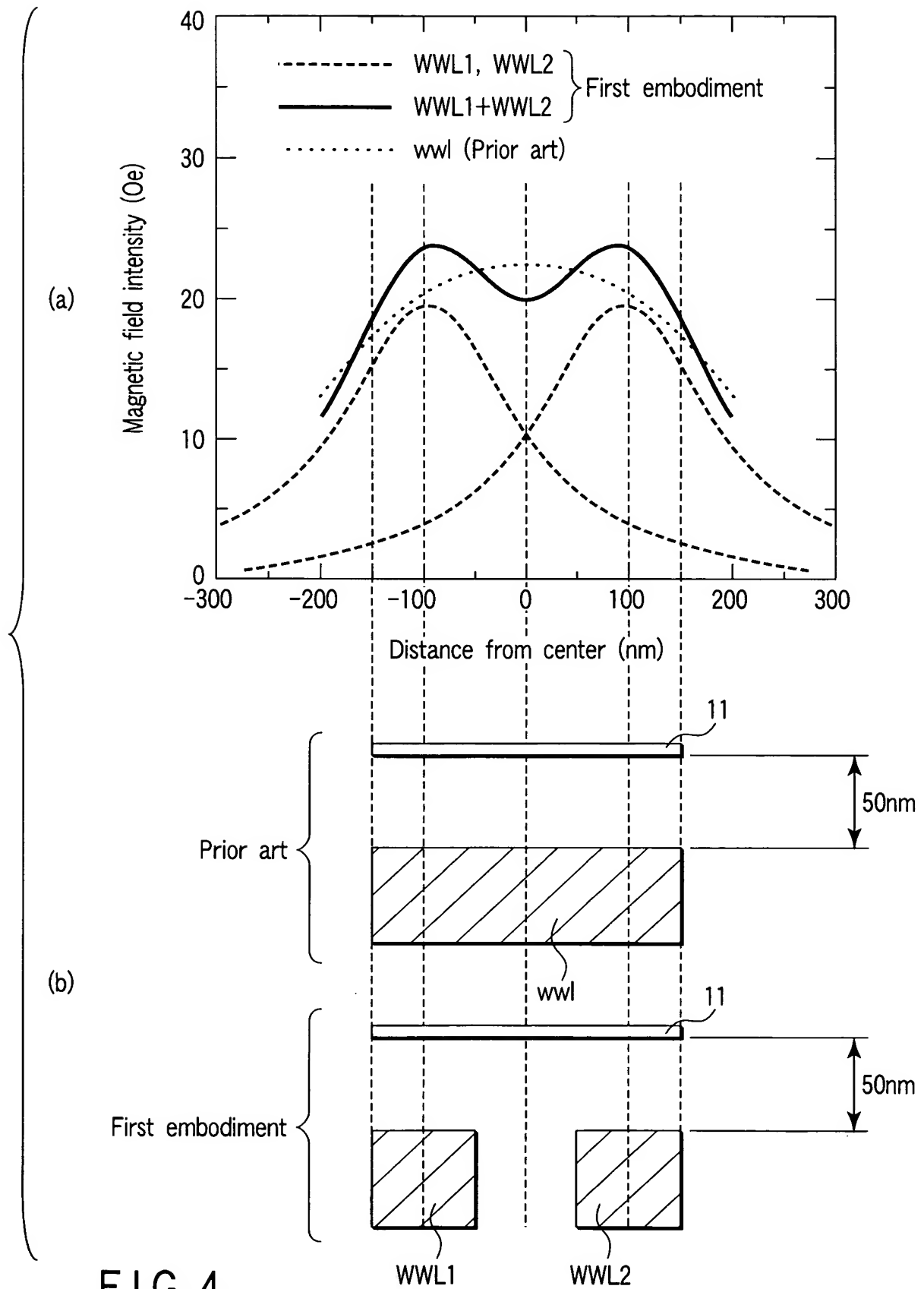


FIG. 4

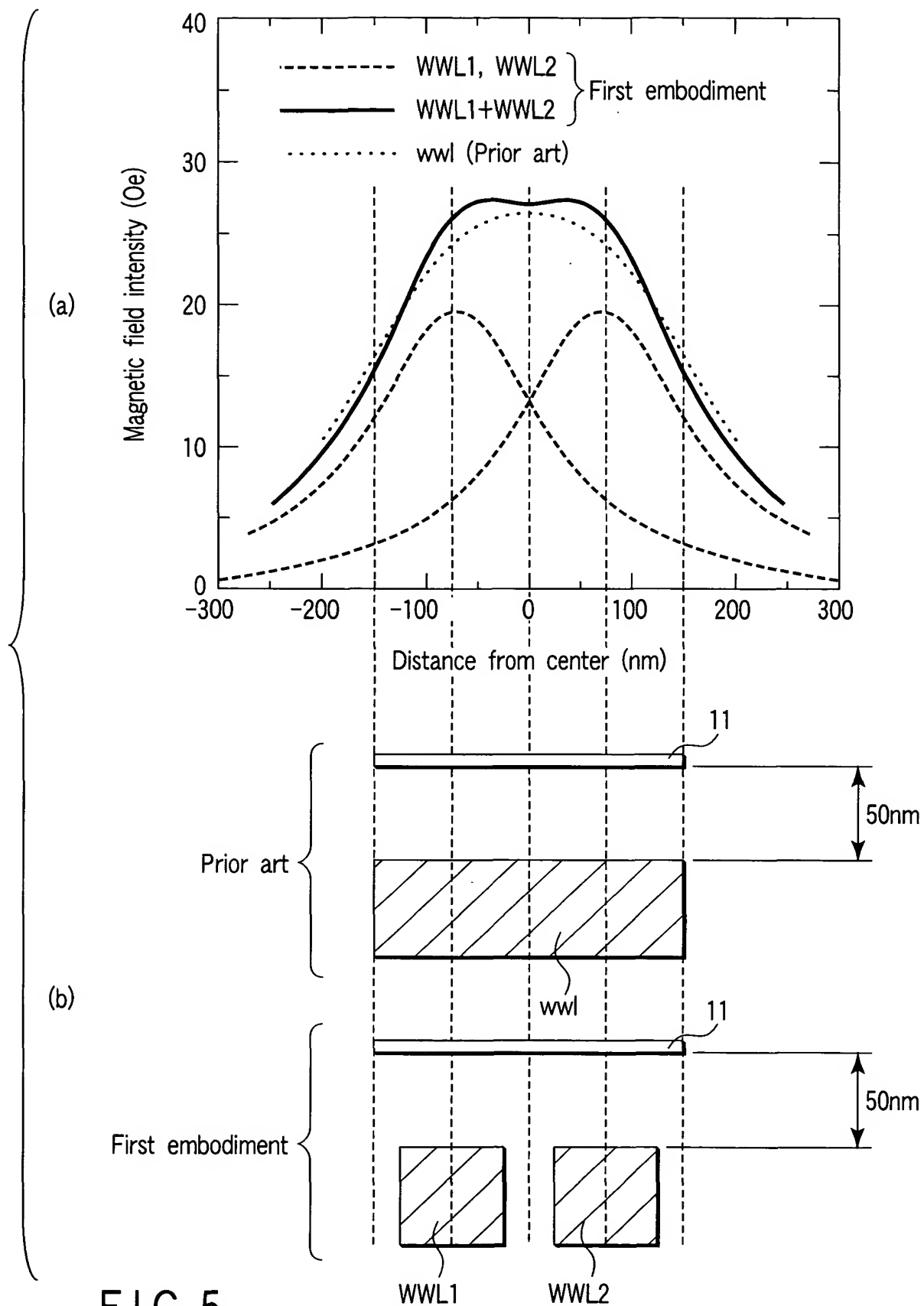


FIG. 5

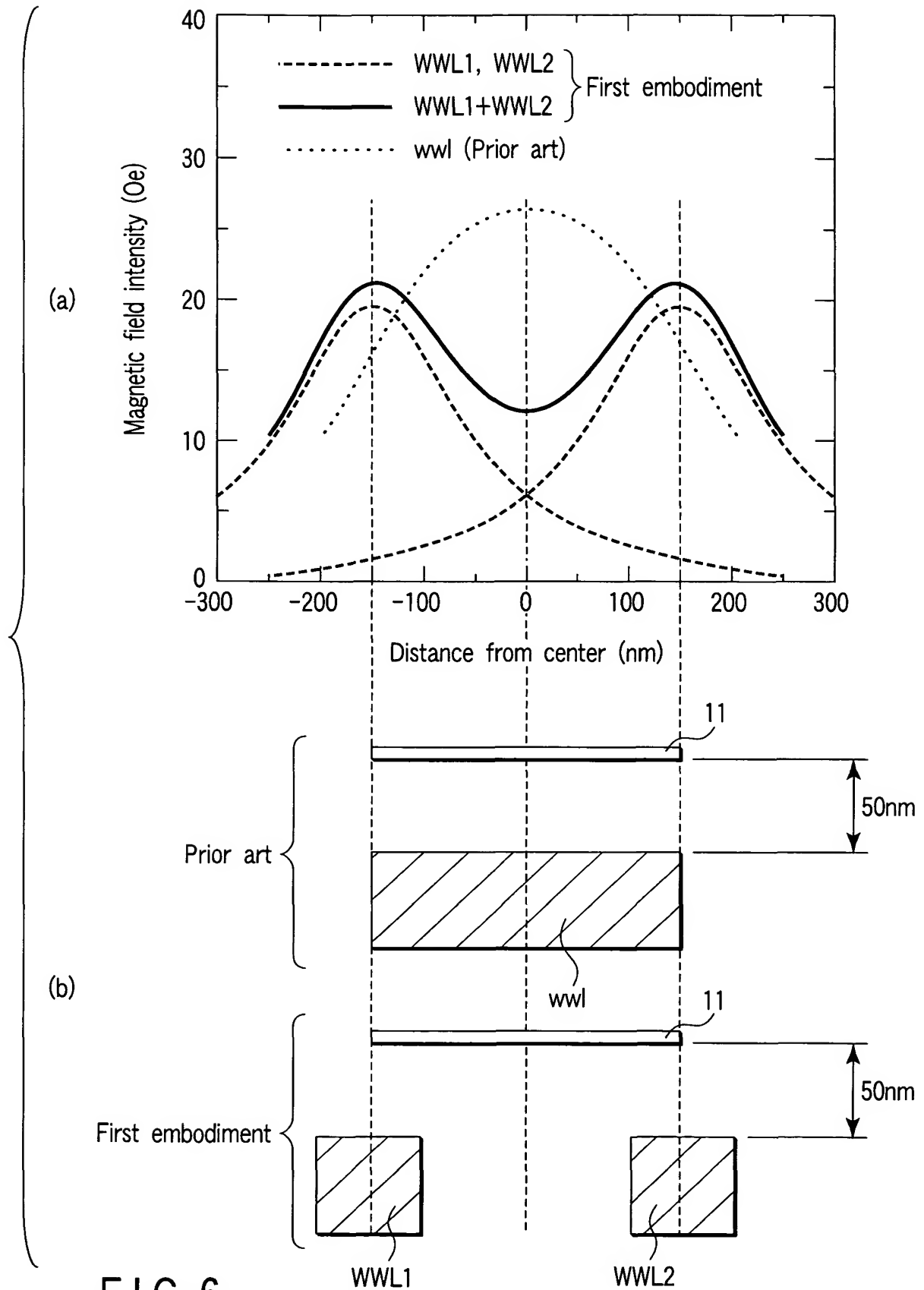


FIG. 6

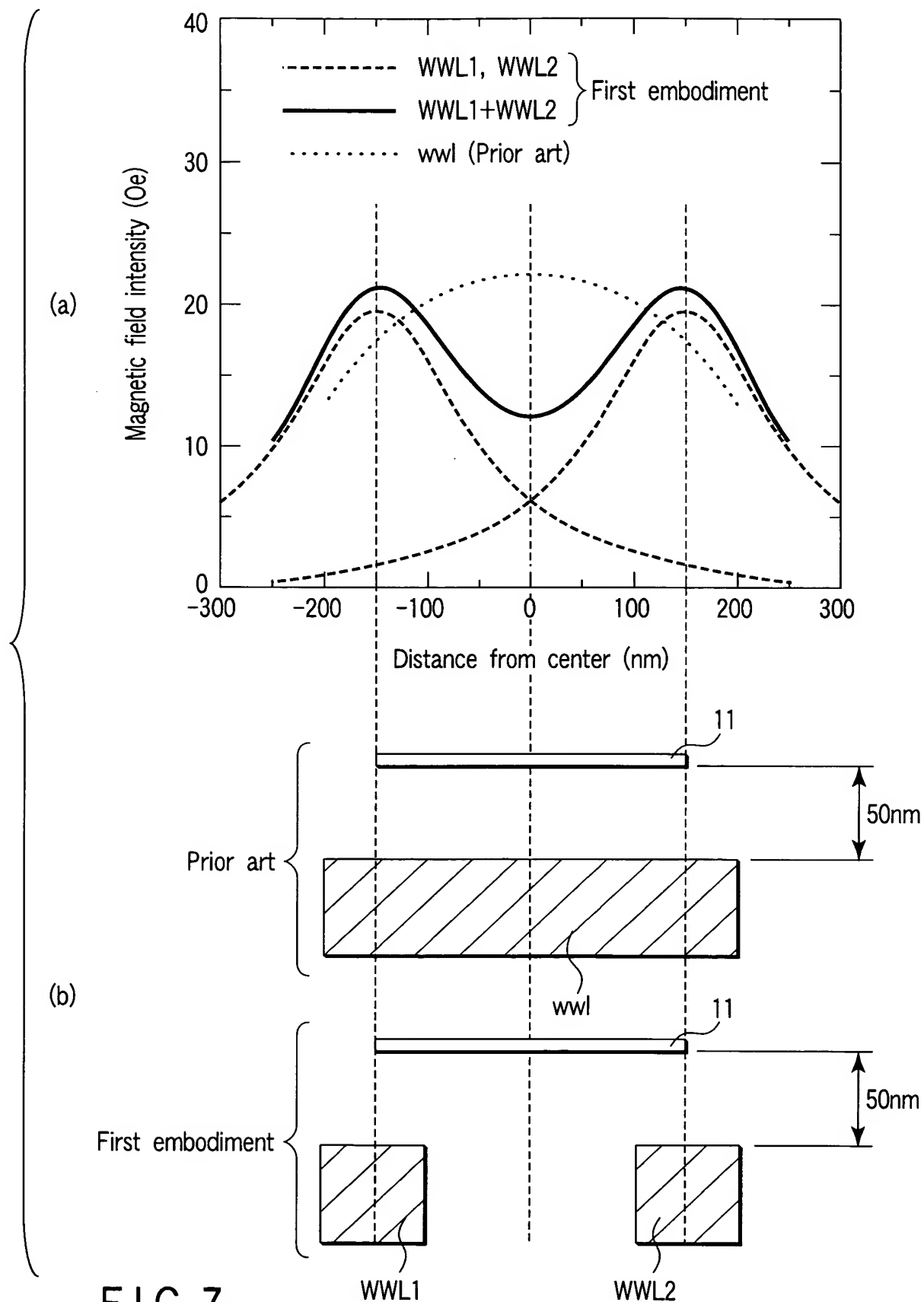


FIG. 7

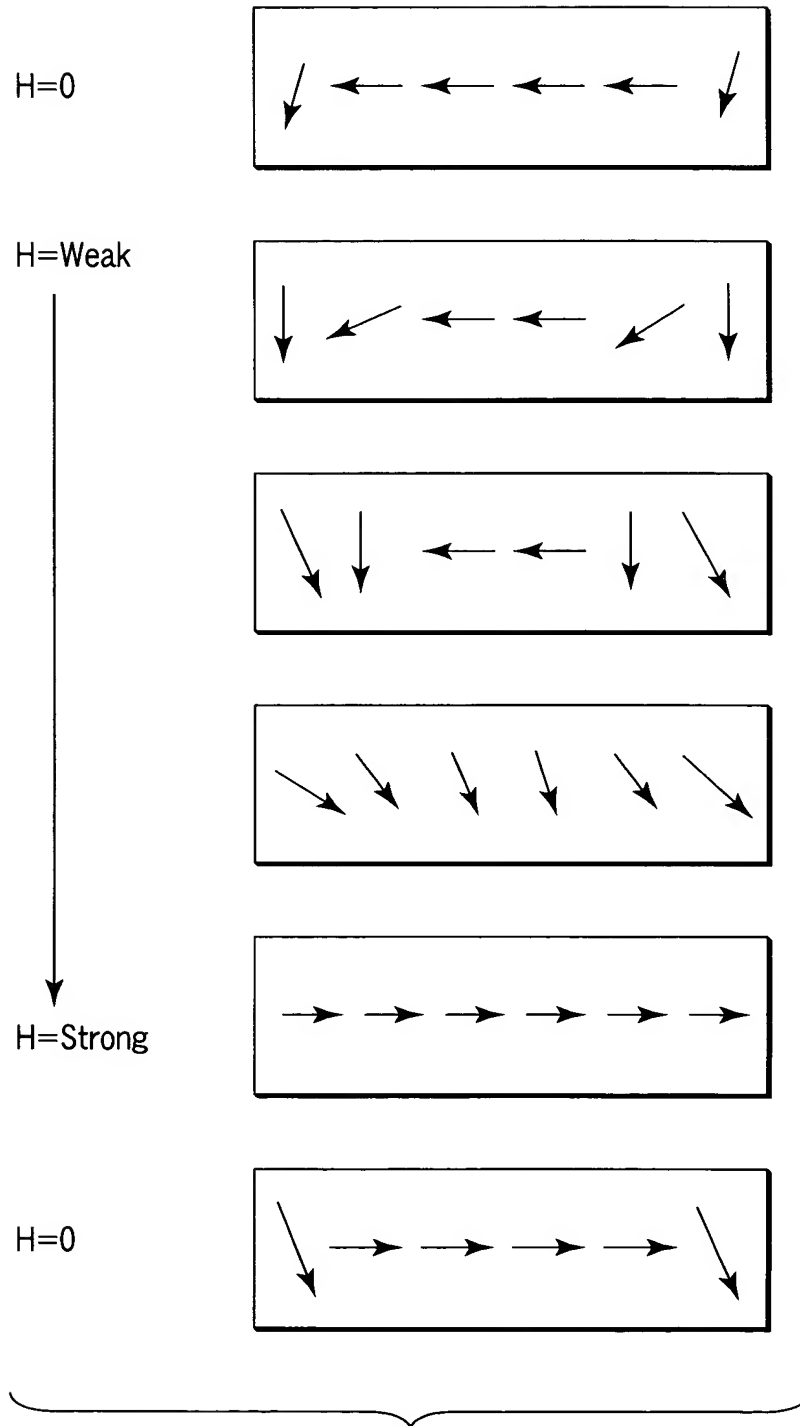


FIG. 8

FIG. 10

FIG. 10

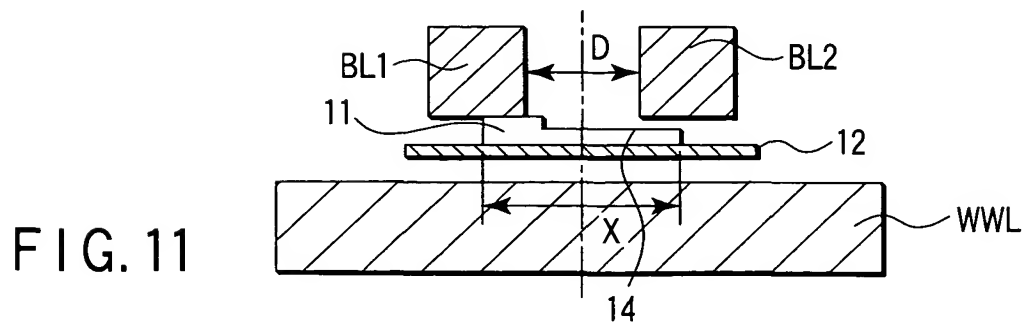


FIG. 13

Memory cell region

Peripheral circuit region

Diagram illustrating a cross-sectional view of a semiconductor device. A substrate (BL) is shown with a gate line (11) and word lines (WWL1, WWL2). A distance X is indicated between the gate line and the word lines. A distance D is indicated between WWL1 and WWL2. A contact (13) is shown connecting the gate line to a vertical structure.

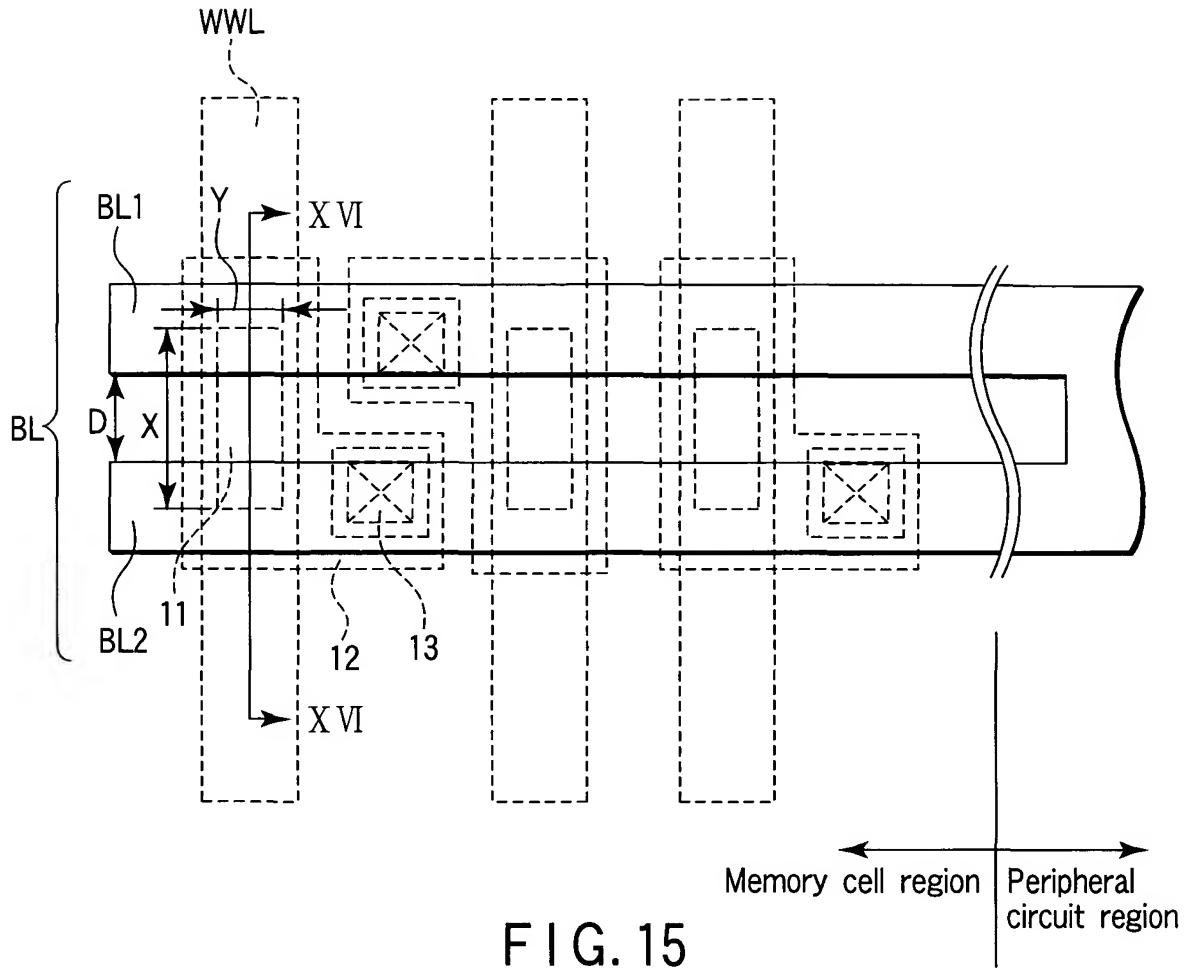


FIG. 15

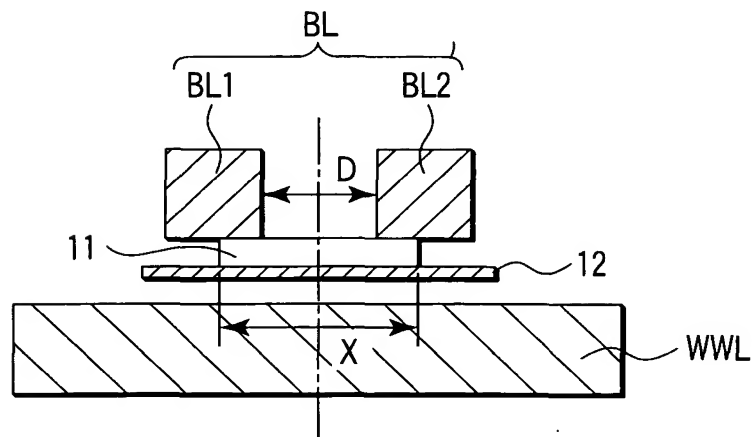


FIG. 16

FIG. 18

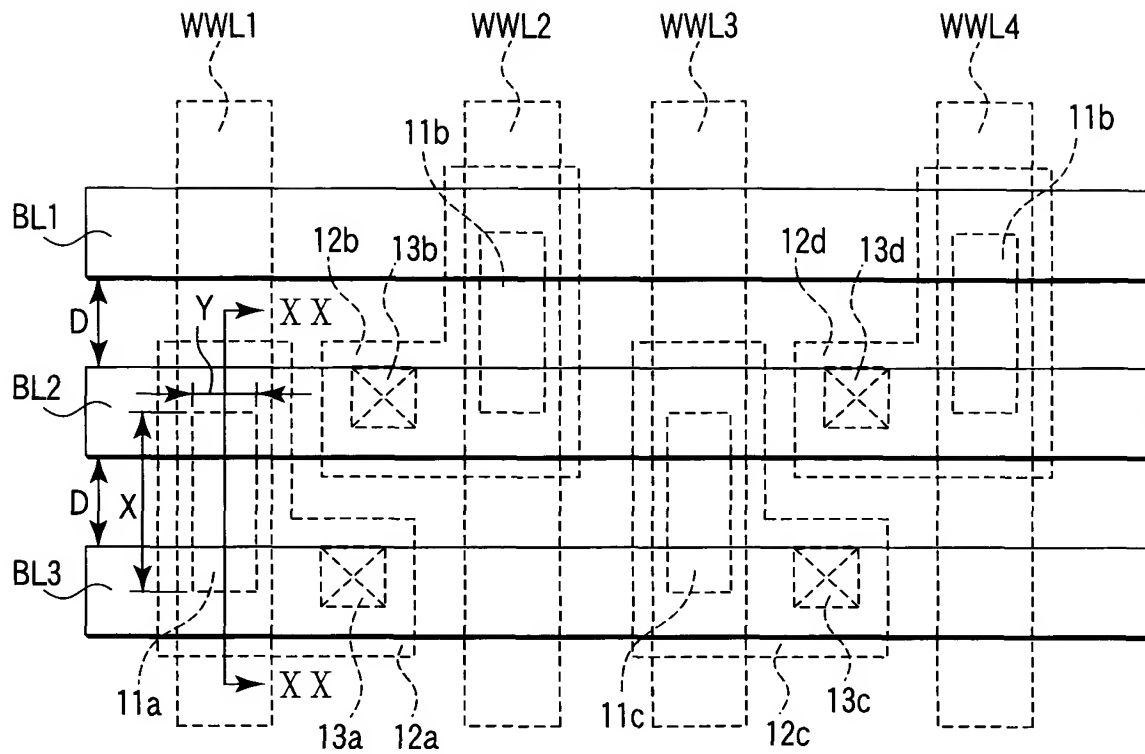


FIG. 19

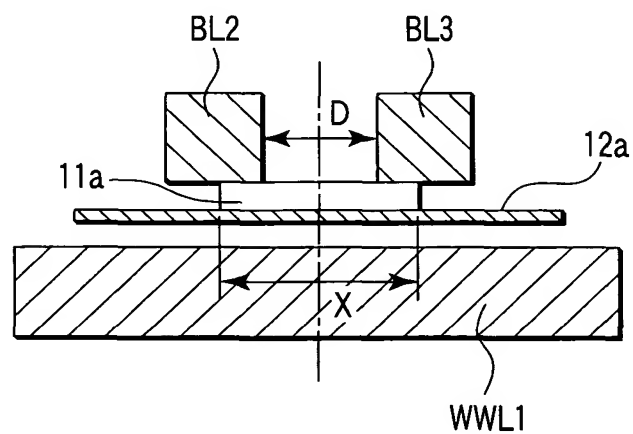


FIG. 20

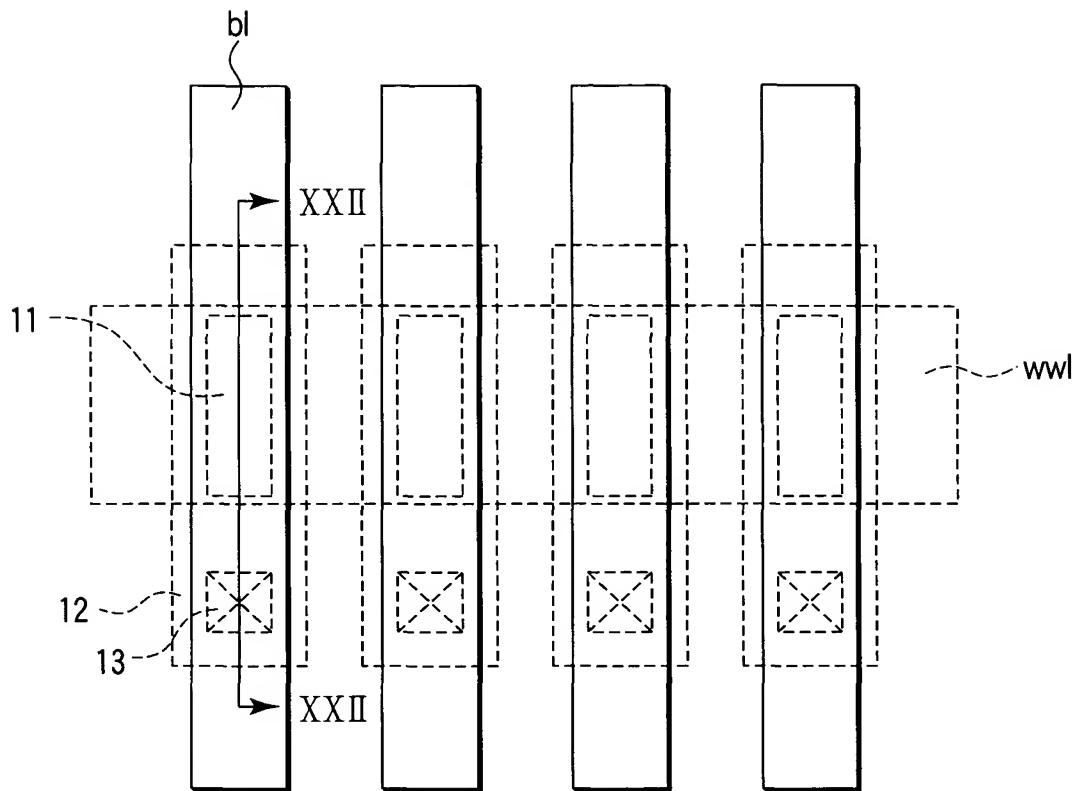


FIG. 21 PRIOR ART

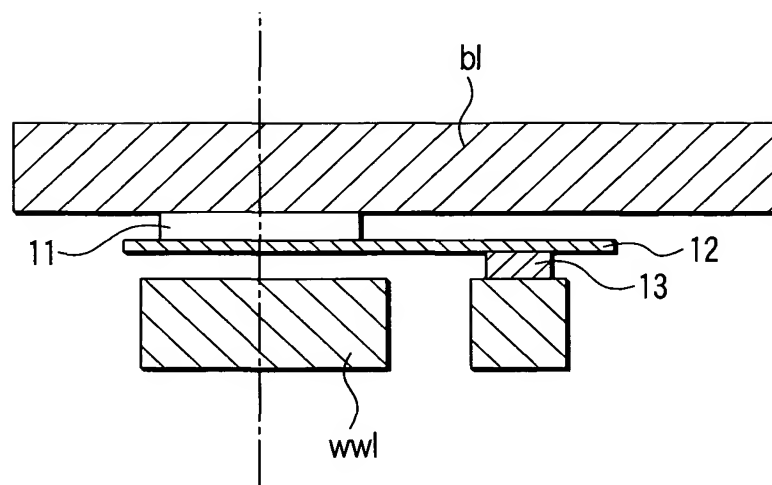


FIG. 22 PRIOR ART